Polycrystalline $Ba_{0.6}Sr_{0.4}TiO_3$ thin films on *r*-plane sapphire: Effect of film thickness on strain and dielectric properties

E. A. Fardin,[a] A. S. Holland, and K. Ghorbani
School of Electrical and Computer Engineering, RMIT University, Melbourne, Victoria 3001, Australia

E. K. Akdogan, W. K. Simon, and A. Safari
Department of Materials Science and Engineering, Rutgers-The State University of New Jersey, Piscataway, New Jersey 08854

J. Y. Wang
Centre for Atom Optics and Ultrafast Spectroscopy, ARC Centre of Excellence for Quantum-Atom Optics, Swinburne University of Technology, Hawthorn, Victoria 3122, Australia

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Polycrystalline $Ba_{0.6}Sr_{0.4}TiO_3$ (BST) films grown on *r*-plane sapphire exhibit strong variation of in-plane strain over the thickness range of 25–400 nm. At a critical thickness of ~200 nm, the films are strain relieved; in thinner films, the strain is tensile, while compressive strain was observed in the 400 nm film. Microwave properties of the films were measured from 1 to 20 GHz by the interdigital capacitor method. A capacitance tunability of 64% was observed in the 200 nm film, while thinner films showed improved Q factor. These results demonstrate the possibility of incorporating frequency agile BST-based devices into the silicon on sapphire process. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2374810]

Barium strontium titanate (BST hereafter) thin films are promising candidates for the realization of reduced size dc blocking capacitors[1] and varactors for reconfigurable microwave circuits.[2,3] One of the challenges, which have so far limited the implementation of BST in commercial radio frequency integrated circuits (RFICs hereafter), is the poor compatibility of BST with conventional semiconductor processes. A significant problem is the high deposition temperatures (typically 650–800 °C) required to form the paraelectric perovskite phase of BST. In the parallel-plate capacitor architecture, it has been shown that platinum bottom electrodes on silicon are prone to hillock formation, leading to short circuit devices.[4] Furthermore, the low resistivity of silicon makes the realization of low loss microwave transmission lines and passive components on silicon challenging.

Silicon on sapphire (SoS hereafter) technology presents a possible solution to the integration of BST with semiconductor devices. In the SoS process, a thin (~0.5 μm) heteroepitaxial layer of Si is deposited on an *r*-plane sapphire substrate. Although high tunability BST films grown on *c*-plane sapphire have been reported,[5] this substrate orientation is not suitable for the growth of silicon on sapphire. The main advantage of SoS over traditional bulk Si integrated circuits is the high isolation between devices, which allows higher operating speed and lower power dissipation, and also minimizes the formation of parasitic semiconductor junctions.[6] Sapphire has excellent microwave properties compared to silicon, with a loss tangent $\tan\delta < 10^{-4}$ at 3 GHz and resistivity $\rho = 10^{14}\ \Omega$ cm (Ref. 7). This allows the formation of improved Q-factor on-chip inductors, thus overcoming a significant problem in bulk Si-based RFIC. By depositing a BST layer on sapphire early in the SoS process (before contact metallization), the high temperatures can be tolerated without affecting the Si epilayer. Therefore, the advantages of SoS and tunable BST-based components can be combined to realize high performance RFICs.

Li *et al.* have demonstrated high tunability $Ba_{0.5}Sr_{0.5}TiO_3$ thin films on SiO_2 on *r*-plane sapphire.[2] The BST film was grown on Si/Al_2O_3, and the underlying Si layer was converted to amorphous SiO_2 by annealing at 1000 °C for 48 h in an oxygen atmosphere. The microwave properties of $Ba_{0.65}Sr_{0.35}TiO_3$ films grown on *r*-plane sapphire with a $SrTiO_3$ buffer layer have also been reported by Hollmann *et al.*[8] Recently, the properties of a 1 μm thick BST film deposited by rf magnetron sputtering on *r*-plane sapphire were investigated and compared to identical films on MgO, Si, and *c*/*r*-plane sapphire substrates.[9] However, there has been no comprehensive investigation into the thickness dependent properties of BST films grown directly on *r*-plane sapphire.

In this study, we investigate the properties of $Ba_{0.60}Sr_{0.40}TiO_3$ (BST 60/40 hereafter) films grown on *r*-plane sapphire by pulsed laser deposition (PLD). A KrF excimer laser ($\lambda = 248$ nm) with 2 J/cm^2 fluence and 2 Hz repetition rate was used for the experiments. Prior to deposition, the substrates were *in situ* annealed in flowing oxygen for 60 min at 100 mTorr, in order to remove organic contaminants from the film surface.[10] The substrate temperature was 700 °C and the oxygen pressure in the chamber was 100 mTorr during deposition. All of the samples were post-deposition annealed inside the chamber at 700 °C under 1 atm oxygen pressure for 6 h before cooling to room temperature. Interdigital capacitors (IDCs hereafter) with adjacent open and short-circuit calibration standards were fabricated on the film surface by e-beam evaporation of a Ti/Ni/Au seed layer and electroplating of 2.5 μm Au, respectively.[5] The finger width, finger spacing, and finger end gap were 5 μm, 2 μm, and 10 μm, respectively. For different devices, the finger overlap length ranged from 80 to 100 μm. To enable probing in the ground-signal-

[a]Electronic mail: efardin@ieee.org

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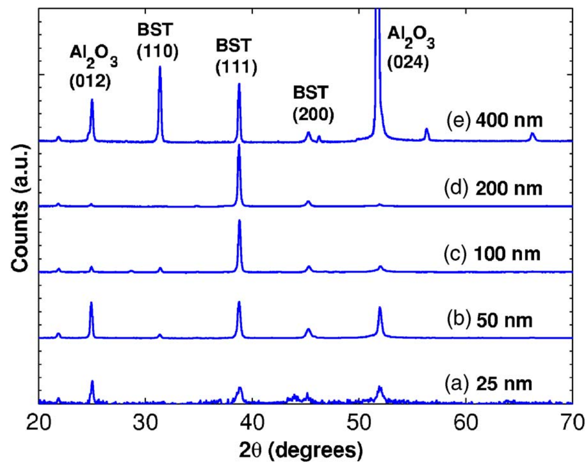

FIG. 1. (Color online) X-ray diffraction (XRD) patterns for polycrystalline BST thin films of thickness 25–400 nm on *r*-plane sapphire.

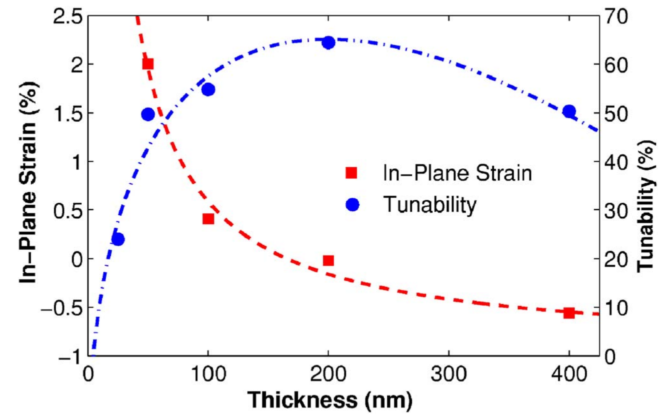

FIG. 2. (Color online) In-plane strain and capacitance tunability as a function of film thickness. The measured values and trend lines are represented by points and dashed lines, respectively.

ground configuration, the IDCs were designed with two sets of eight interdigital fingers.

Atomic force microscopy was used to assess the surface roughness and grain size of the films. The average roughness parameter (R_a) varied from 2.2 nm in the thinnest (25 nm) film to 8.2 nm in the thickest (400 nm) film, which are consistent with epitaxial BST films deposited on MgO, $LaAlO_3$, and $NdGaO_3$ substrates using similar PLD parameters.[11–13] It was found that the grain size increased with film thickness, from ~50 nm in the 25 nm film to ~100 nm in the 400 nm film.

Qualitative x-ray phase analysis indicated that films of all thicknesses were single phase and polycrystalline. Epitaxial film growth is precluded since the *r*-plane sapphire does not provide a lattice-matched growth surface for BST. Furthermore, it was found that the films are increasingly ⟨111⟩ oriented by monitoring the intensity of the (111) reflection as the thickness increases from 25 to 200 nm, as shown in Figs. 1(a)–1(d). However, in Fig. 1(e) a strong ⟨110⟩ BST peak is evident for the 400 nm film, indicating that the texture becomes bimodal at higher thicknesses in such polycrystalline BST films.

Many reports have demonstrated a link between tunability and strain in BST thin films, both experimentally[13–15] and theoretically.[16] High tunability is typically achieved when the residual stress in the film is vastly relaxed as the film thickness is increased.[13–15] It has also been suggested that small grain size, which leads to greater grain boundary area, and the associated interfacial capacitance are major contributing factors to the lower permittivity observed in BST thin films relative to bulk ceramics of the same composition.[17]

The x-ray diffraction (XRD) $\sin^2\psi$ technique[18] was employed to determine the effect of the film thickness on the in-plane strain. Scans performed in two mutually perpendicular in-plane directions ($\varphi=0^\circ,90^\circ$) revealed no significant difference in the slope of the d-$\sin^2\psi$ characteristic traces. Therefore, both the in-plane and perpendicular shear stress components were inferred to be zero, resulting in an equal biaxial state of stress in the 50–200 nm films.[19] Using the linear theory of elasticity in conjunction with elasticity data[20] for BST 60/40, the in-plane strains were computed, as depicted in Fig. 2. For the series of films, the strain was calculated according to[19]

$$\frac{d_\psi - d_0}{d_0} = \sigma\left(\frac{2s_{11}+4s_{12}-s_{44}}{3} + \frac{s_{44}}{2}\sin^2\psi\right), \tag{1}$$

where d_ψ is the measured interplanar spacing, d_0 is the unstrained lattice parameter, and s_{ij} are elastic compliances. The tensile residual misfit strain varies from 2.0% at 50 nm film thickness to ~0.5% at 100 nm, followed by a decrease to ~0% at 200 nm. Films greater than 200 nm in thickness are under a compressive state of strain, which reaches a magnitude of −0.6% at 400 nm. No strain data for the 25 nm film are reported herein due to the lack of a sufficiently strong high-angle diffraction peak suitable for stress measurement.

Single port (S_{11}) measurements from 1 to 20 GHz were used to extract the capacitance of the IDCs as a function of bias voltage. The parasitic component values associated with the pad metallization were calculated using open and short-circuit calibration standards next to each IDC, in order to accurately determine the capacitance and Q factor of the device.[21] A final capacitance value was calculated by averaging the frequency dependent extracted capacitance from 1 to 20 GHz. The maximum dc bias applied to the IDCs was 40 V, corresponding to a bias field of 200 kV cm^{-1}. A high capacitance tunability of 64%, calculated as $[C(0)-C(40)]/C(0)$, was observed in the 200 nm film. In the same device, a zero-bias Q factor of ~8 at 10 GHz was calculated using a series RC circuit to model the BST varactor.[21] The lowest tunability and best Q factor of the series (24% and ~23% at 10 GHz, respectively) were observed in the 25 nm film. A summary of the IDC capacitance and Q-factor variation with film thickness is shown in Fig. 3. Comparing the variation of tunability with the variation of residual misfit strain (Fig. 2), one observes that it scales inversely with the magnitude of the strain and not its sign, i.e., the lower the strain the higher the tunability. The observed behavior parallels the one observed in epitaxial films,[11–15] which indicates that the strain effect on tunability is indeed a universal phenomenon. Therefore, we arrive at the conclusion that the polycrystalline (as opposed to epitaxial) nature of the films does not affect the overall strain dependence of tunability in paraelectric BST.

The dielectric permittivity ε_r of the films was determined by conformal mapping of the capacitance data according to the formalism proposed by Gevorgian et *al.*[22] An approximation for the elliptic integral argument [Eq. (14) of Ref. 22] was applied to avoid numerical problems in the

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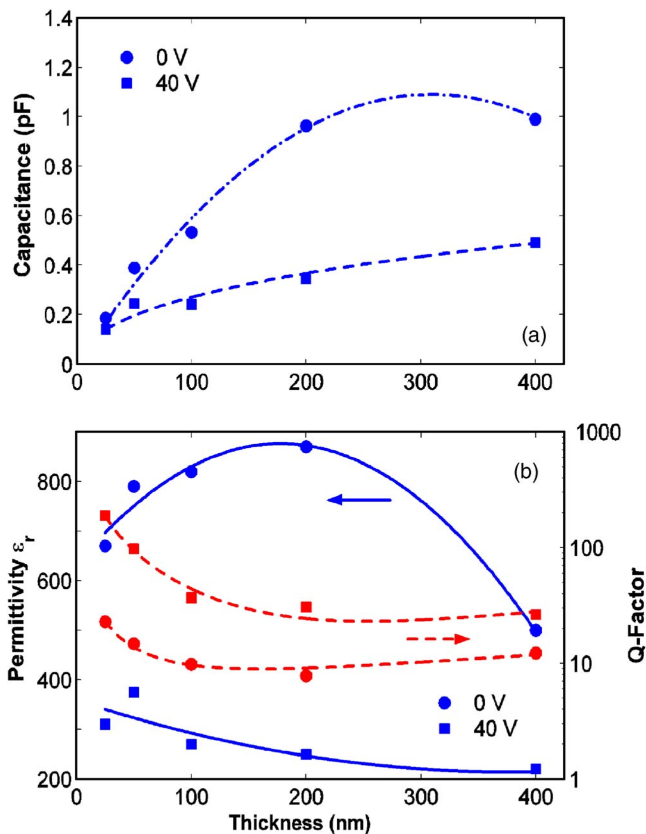

FIG. 3. (Color online) Thickness dependence of (a) IDC capacitance and (b) in-plane dielectric permittivity ε_r and Q factor of the BST films at 0 and 40 V dc biases. The measured values and trend lines are represented by points and dashed lines, respectively.

analysis of the ultrathin 25 nm film. As shown in Fig. 3(b), the maximum permittivity ($\varepsilon_r \sim 870$) occurs at around 200 nm film thickness. In the thinner films, ε_r decreases due to higher tensile strain and reduced grain size. A reduced ε_r was also observed in the 400 nm film, while the film is under a compressive state of strain ($\sim -0.6\%$), and has a larger grain size relative to the 50–100 nm films. This strain state of the 400 nm film is attributed to the thermal expansion coefficient (TEC) mismatch between the substrate and the film. Noting that the dislocation slip system is $\{101\}\langle 10\bar{1}\rangle$ in perovskites,[23] the development of strong $\langle 110\rangle$ texturing in the 400 nm film should in principle be due to the TEC mismatch-induced loss of crystallographic coherence arising from shear stresses on $\{110\}$ planes and in $\langle 110\rangle$ directions.

In summary, we have presented the thickness dependent dielectric properties of polycrystalline BST (60/40) films on r-plane sapphire. A strain relaxation was observed at around 200 nm film thickness, resulting in high dielectric tunability. A trade-off between tunability and Q factor can be achieved by reducing the film thickness. These results demonstrate the possibility for integration of BST with SoS technology. Since the maximum temperature reached during the deposition and heat treatment of the BST film is 700 °C, it is unlikely that the process would degrade the properties of semiconductor devices on the same wafer, provided that the BST deposition was done before interconnect metallization.

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[1] H. Xu, N. K. Pervez, P. J. Hansen, L. Chen, S. Keller, U. K. Mishra, and R. A. York, IEEE Electron Device Lett. **25**, 49 (2004).
[2] H. Li, J. Finder, Y. Liang, R. Gregory, and W. Qin, Appl. Phys. Lett. **87**, 072905 (2005).
[3] D. Ghosh, B. Laughlin, J. Nath, A. I. Kingon, M. B. Steer, and J.-P. Maria, Thin Solid Films **496**, 669 (2006).
[4] S. R. Summerfelt, D. Kotecki, A. Kingon, and H. N. Al-Shareef, Mater. Res. Soc. Symp. Proc. **361**, 257 (1995).
[5] E. A. Fardin, A. S. Holland, and K. Ghorbani, Appl. Phys. Lett. **89**, 022901 (2006).
[6] S. Cristoloveanu, Rep. Prog. Phys. **50**, 327 (1987).
[7] R. A. Johnson, P. R. de la Houssaye, C. E. Chang, P.-F. Chen, M. E. Wood, G. A. Garcia, I. Lagnado, and P. M. Asbeck, IEEE Trans. Electron Devices **45**, 1047 (1998).
[8] E. K. Hollmann, V. I. Gol'drin, V. E. Loginov, A. M. Prudan, and A. V. Zemtsov, Tech. Phys. Lett. **25**, 549 (1999).
[9] G. Bhakdisongkhram, Y. Yamashita, T. Nishida, and T. Shiosaki, Jpn. J. Appl. Phys., Part 1 **44**, 7098 (2005).
[10] J. A. Bellotti, Ph.D. thesis, Rutgers-The State University of New Jersey, 2003.
[11] J. A. Bellotti, E. K. Akdogan, A. Safari, W. Chang, and S. K. Kirchoefer, Integr. Ferroelectr. **49**, 113 (2002).
[12] J. Bellotti, E. K. Akdogan, and A. Safari, Ferroelectrics **271**, 131 (2002).
[13] W. K. Simon, E. K. Akdogan, A. Safari, and J. A. Bellotti, Appl. Phys. Lett. **87**, 082906 (2005).
[14] W. K. Simon, E. K. Akdogan, and A. Safari, Appl. Phys. Lett. **89**, 022902 (2006).
[15] W. K. Simon, E. K. Akdogan, and A. Safari, J. Appl. Phys. **97**, 103530 (2005).
[16] Z.-G. Ban and S. P. Alpay, J. Appl. Phys. **93**, 504 (2003).
[17] T. M. Shaw, Z. Suo, M. Huang, E. Liniger, R. B. Laibowitz, and J. D. Baniecki, Appl. Phys. Lett. **75**, 2129 (1999).
[18] I. C. Noyan and J. B. Cohen, *Residual Stress* (Springer, Berlin, 1987), p. 122.
[19] B. M. Clemens and J. A. Bain, Mater. Res. Bull. **17**, 46 (1992).
[20] Z.-G. Ban and S. P. Alpay, J. Appl. Phys. **91**, 9288 (2002).
[21] B. Acikel, Ph.D. dissertation, University of California at Santa Barbara, 2002.
[22] S. S. Gevorgian, T. Martinsson, P. L. J. Linnér, and E. L. Kollberg, IEEE Trans. Microwave Theory Tech. **44**, 896 (1996).
[23] J. S. Speck and W. Pompe, J. Appl. Phys. **76**, 466 (1994).

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